IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Sub B14

Claim 1 (Currently Amended): An electrically rewritable nonvolatile semiconductor memory device comprising:

a plurality of memory circuits, each of which has a control circuit for sequentially controlling writing, provided ~~in~~ on a memory chip so as to share a data bus, and

~~a chip enable terminal~~ a plurality of chip enable terminals for controlling the activity and inactivity of ~~each of the memory circuits provided~~ the memory circuits, respectively provided for each of the memory circuits; and

a master chip enable terminal for controlling the activity and inactivity of said memory chip as a whole, the activity and inactivity of each of said memory circuits being controlled by a logical output of a signal of said master chip enable terminal;

wherein each of said memory circuits is provided with a ready/busy signal terminal which corresponds to a respective chip enable terminal.

Claim 2 (Canceled).

Claim 3 (Canceled).

Claim 4 (Currently Amended): The electrically rewritable nonvolatile semiconductor memory device as set forth in claim ~~3~~ 1, wherein said logical output is an output of an AND gate ~~where~~ having the signal of said master chip enable terminal and the signal of ~~the each~~ a respective chip enable terminal ~~are applied~~ as inputs.

Claim 5 (Currently Amended): An electrically rewritable nonvolatile semiconductor memory device ~~having~~ comprising a plurality of memory circuits, each of which has a control circuit for sequentially controlling writing, provided ~~in~~ on a memory chip so as to share a data bus,

wherein the activity and inactivity of each of the memory circuits are controlled by inputting a command.

Claim 6 (Currently Amended): The electrically rewritable nonvolatile semiconductor memory device as set forth in claim 5, wherein a common chip enable terminal is provided for said plurality of memory circuits, and an enable signal inputted to said common chip enable terminal is supplied to a selected one of said memory circuits which has been selected by inputting said command.

Claim 7 (Canceled).

Claim 8 (Currently Amended): The electrically rewritable nonvolatile semiconductor memory device as set forth in claim 6, wherein a common ready/busy signal terminal is provided for said plurality of memory circuits, and a ready/busy state of said selected one of said memory circuits, which has been selected by inputting said command, is outputted to said common ready/busy signal terminal.

Claim 9 (Currently Amended): An electrically rewritable nonvolatile semiconductor memory device ~~wherein~~ comprising a plurality of memory circuits~~, which are able to assign an address, are~~ provided in a memory chip, ~~and~~ each of said memory circuits ~~is provided with~~ including a corresponding at least one ~~stage of~~ data buffer stage for transmitting writing data

corresponding to ~~said~~ an address, and wherein writing operations in said plurality of memory circuits are simultaneously carried out ~~via said data buffer~~ and a pass/fail result of each of said writing operations is output to each of said memory circuits and stored in the corresponding at least one data buffer stage.

Claim 10 (Canceled).

Claim 11 (Canceled).

Claim 12 (Canceled).

Claim 13 (Currently Amended): ~~The~~ An electrically rewritable nonvolatile semiconductor memory device comprising: ~~as set forth in claim 10, which has,~~

a plurality of memory circuits provided in a memory chip, each of said memory circuits ~~is~~ including a corresponding at least one data buffer stage for transmitting writing data corresponding to an address, and wherein writing operations in said plurality of memory circuits are simultaneously carried out and a pass/fail result of each of said writing operations is output to each of said memory circuits;

wherein ~~a mode in which~~ it is determined whether data ~~are~~ is able to be inputted to said at least one data buffer stage by referring to said pass fail result, and a mode in which it is determined whether data ~~are~~ is able to be ~~inputted~~ input to said data buffer without referring to said pass/fail result.

Claim 14 (Canceled).

Claim 15 (New): The electrically erasable nonvolatile semiconductor of Claim 1, wherein each of said memory circuits has a stacked gate structure.

Claim 16 (New): The electrically erasable nonvolatile semiconductor of Claim 9, wherein each of said memory circuits has a stacked gate structure.

Claim 17 (New): The electrically erasable nonvolatile semiconductor of Claim 13, wherein each of said memory circuits has a stacked gate structure.

Claim 18 (New): The electrically erasable nonvolatile semiconductor of Claim 15, wherein said stacked gate structure is a NAND structure.

Claim 19 (New): The electrically erasable nonvolatile semiconductor of Claim 16, wherein said stacked gate structure is a NAND structure.

Claim 20 (New): The electrically erasable nonvolatile semiconductor of Claim 17, wherein said stacked gate structure is a NAND structure.